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removing the layer of photo resist prior to the step of selectively etching the dielectric layer through the germanium hard mask

REMARKS

Claims 1-20 are currently pending and stand rejected. Applicants have amended claims 1, 9 and 15, and have added new claim 21. No new matter was added. Applicants request reconsideration of the application as amended in light of the following remarks.

Objections to the Drawings

The Drawings were objected to for failing to show every feature of the invention specified in the claims. In response to the objection, Applicants added new drawings 7 and 8. Figure 7 includes an etched portion of the semiconductor substrate, and Figure 8 includes dielectric and conductive structures over the semiconductor substrate. Independent claims 1, 9 and 15 were amended so that the feature of "forming a dielectric layer" is not recited. The features shown in the new drawings are supported by the specification, page 6, line 25 to page 7, line 3, and by originally filed claims 1, 9, 15 and 18. Additionally, etching a substrate and forming structures over the substrate, as explained in Applicants' specification, are well known in the art. Applicants request that the Examiner admit new Figures 7 and 8 provided herewith and withdraw the objection to the Drawings.

Obviousness Rejections under 35 U.S.C. § 103(a)

Claims 1-20 were rejected by the Examiner under 35 U.S.C. § 103(a) as being unpatentable over Cho, et al. (U.S. Patent No.6,074,930-A, hereinafter "Cho") in view of Juengling (U.S. Patent No. 5,750,442, hereinafter "Juengling"). Applicants respectfully traverse this rejection.

Applicants submit that to establish a *prima facie* case of obviousness under 35 U.S.C. § 103, three basic criteria must be met. First, there must be some suggestion or motivation, either in the references themselves or in the knowledge generally available to

one of ordinary skill in the art, to modify the reference or to combine reference teachings. Second, there must be a reasonable expectation of success. Third, the cited prior art reference must teach or suggest all of the claim limitations. Furthermore, the suggestion to make the claimed combination and the reasonable expectation of success must both be found in the prior art, and not based upon Applicants' disclosure. A failure to meet any one of these criteria is a failure to establish a *prima facie* case of obviousness.

Independent Claims 1, 9 and 15

Specifically, independent claims 1, 9 and 15 were rejected over a combination of Cho and Juengling wherein the rejection asserts that Cho discloses each of the claimed elements except "depositing a layer of metallic germanium over the dielectric layer," and "patterning the metallic germanium layer to form a germanium hard mask." The rejection asserts that combining the teachings of Juengling with those of Cho provides the remaining elements. Applicants disagree.

Juengling teaches to deposit a germanium layer over a nitride layer prior to depositing a photo resist layer in order to "substantially reduce reflection from the underlying nitride layer" during exposure of the photo resist layer. *See* Juengling col. 3, lines 42-60 and col. 4, lines 27-32. After the photo resist layer is exposed and developed to form a patterned photo resist layer, the germanium layer merely assists in removing the photo resist residue. The germanium layer and dielectric layers are all etched according to the patterned photo resist layer using an ansiotropic etch. *See Id.* The germanium layer and photo resist layer are then completely removed before the semiconductor substrate is processed. *See* Juengling col. 3, line 60 to col. 4, line 17. The teachings of Juengling relating to a germanium layer, therefore, are only to enhance the photo resist process and are apparently irrelevant to the actual etching of the semiconductor substrate.

A hard mask is a patterned layer which is used to protect portions of one or more layers beneath the hard mask layer while other portions of the layers beneath are selectively etched. The germanium layer of Juengling is completely removed prior to etching any of the

lower layers. *Id.* Therefore, there is no teaching or suggestion in the disclosure of Juengling to use the germanium layer as a hard mask.

Cho teaches that a photo resist layer should be placed over a silicon dioxide hard mask layer 36 which is above a silicon nitride layer 34. *See* Cho col. 3, line 61 to col. 4, line 3. The photo resist layer is then patterned prior to dry etching the hard mask and the dielectric layer to expose portions of the semiconductor substrate. *See* Cho col. 4, lines 4-22. An ashing/strip process is used to remove the photo resist prior to processing the semiconductor substrate. *See* Cho col. 4, lines 22-24.

It would not be obvious to combine the teachings of Juengling with the teachings of Cho. Juengling teaches that the scope of its invention involving the germanium layer added below the photo resist relates to "semiconductor processing steps in which a wafer having a nitride top layer is to be patterned by photolithography." *See* Juengling col. 4, lines 33-35. The top layer of Cho is not a nitride layer, but a silicon dioxide layer. *See* Cho col. 3, line 67 to col. 4, line 3. Therefore, there is no teaching or suggestion to add the germanium layer of Juengling between the silicon dioxide layer and the photo resist layer of Cho.

Furthermore, even if there were a teaching or suggestion to place the germanium layer of Juengling below the photo resist layer of Cho, the proposed combination would not result in the novel inventions claimed by Applicants in claims 1, 9 and 15. Claim 1 recites "patterning the layer of metallic germanium to form the germanium hard mask . . . ." If the germanium layer of Juengling were included in the structure of Cho to assist in the photo resist process, there is still no teaching in either Juengling or Cho to "pattern" the layer of germanium or to form a "germanium hard mask." Therefore, claim 1 is not obvious in view of the combination of the teachings of Cho and Juengling. For these same reasons, claim 9 which recites, "patterning the metallic germanium layer to form a germanium hard mask," is also not obvious. Similarly, claim 15 which recites, "forming a germanium hard mask over the dielectric stack" is not obvious because neither Juengling nor Cho teaches or suggests forming a germanium hard mask. Claims 2-8, 10-14 and 16-21 are allowable, among other

reasons, for respectively depending, directly or indirectly, from allowable base claims. Applicants respectfully request that the rejection of claims 1-20 be withdrawn.

Newly Added Claim 21

Newly added claim 21 is also not obvious in view of the teachings and suggestions of Cho and Juengling, alone or in combination, for reciting "removing the layer of photo resist prior to the step of selectively etching the dielectric layer through the germanium hard mask." Both Cho and Juengling teach to etch the dielectric layer prior to removing the photo resist layer. *See* Cho col. 4, lines 13-21 and Juengling col. 3, lines 51-59. As explained in Applicants' specification, page 5, lines 8-31, in an embodiment of Applicants' invention the photo resist layer is patterned to permit patterning of the germanium layer. In a subsequent etching step, using another etching process, the patterned germanium layer serves as a hard mask for etching the dielectric layers. Because there is no teaching or suggestion in the disclosure of Juengling to use the germanium layer as a hard mask, it would not be obvious to remove the layer of photo resist prior to etching the dielectric layers. The photo resist in both Cho nor Juengling acts as the protecting layer to enable selective etching of lower layers. Combining their teachings would not change this aspect of their inventions. Removal of the photo resist layer prior to etching the lower layers would be contrary to the teachings of both Cho and Juengling. Therefore, newly added claim 21 is independently allowable over the combined teachings of Cho and Juengling.

CONCLUSION

In summary, none of the references cited by the Examiner nor any other known prior art, either alone or in combination, disclose the unique combination of features disclosed in applicant's claims presently on file. For this reason, allowance of all of applicant's claims is respectfully solicited.

The amendments herein added one new dependent claim, resulting in fees due of $18.00. Please deduct this $18.00 fee from deposit account 09-0456. In addition, if any fees, including extension of time fees, are due as a result of this response, please charge IBM Corp Deposit Account No. 09-0456. This authorization is intended to act as a constructive petition for an extension of time, should an extension of time be needed as a result of this response. The examiner is invited to telephone the undersigned if this would in any way advance the prosecution of this case.

Respectfully submitted,

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By 
Kenneth C. Booth
Reg. No. 42,342

SCHMEISER, OLSEN & WATTS LLP
18 East University Drive, #101
Mesa, AZ 85201
(480) 655-0073

VERSION WITH MARKINGS TO SHOW CHANGES MADE

Claim 1. (Amended) A method for etching a semiconductor substrate using a germanium hard mask, the semiconductor substrate having a dielectric layer over a major surface thereof, the method comprising the steps of:

[forming a dielectric layer over a major surface of the semiconductor substrate;]

depositing a layer of metallic germanium over the dielectric layer;

patterning the layer of metallic germanium to form the germanium hard mask;

selectively etching the dielectric layer through the germanium hard a mask to form an opening in the dielectric layer; and

selectively etching the semiconductor substrate through the opening in the dielectric layer.

Claim 2. (Unchanged) The method as claimed in claim 1, further comprising the step of stripping away the layer of metallic germanium after performing the step of selectively etching the dielectric layer.

Claim 3. (Unchanged) The method as claimed in claim 2, the step of stripping away the layer of metallic germanium including the steps of:

oxidizing the layer of metallic germanium to form a layer of germanium oxide therefrom; and

removing the layer of germanium oxide.

Claim 4. (Unchanged) The method as claimed in claim 3, the step of removing the layer of germanium oxide including rising the semiconductor substrate in water.

Claim 5. (Unchanged) The method as claimed in claim 2, the step of stripping away the layer of metallic germanium including stripping away the layer of metallic germanium before performing the step of selectively etching the semiconductor substrate.

Claim 6. (Unchanged) The method as claimed in claim 1, the step of depositing a layer of metallic germanium including depositing the layer of metallic germanium having a thickness between approximately 40 nm and approximately 500 nm.

Claim 7. (Unchanged) The method as claimed in claim 1, the step of patterning the layer of metallic germanium further including the steps of:

depositing a photo resist layer over the layer of metallic germanium;

exposing and developing the photo resist layer to form a photolithography image; and

etching the layer of metallic germanium through the photolithography image.

Claim 8. (Unchanged) The method as claimed in claim 1, the step of forming a dielectric layer further including the steps of:

forming a pad oxide layer having a thickness between approximately 5 nm and approximately 30 nm over the major surface of the semiconductor substrate;

depositing a nitride layer having a thickness between 50 nm and approximately 300 nm over the pad oxide layer; and

depositing a mask oxide layer having a thickness between 800 nm and approximately 3,000 nm over the nitride layer.

Claim 9. (Unchanged) A method for fabricating a semiconductor device <u>having a dielectric stack over a major surface thereof</u>, comprising the steps of:

[forming a dielectric stack over a major surface of a semiconductor substrate;]

depositing a metallic germanium layer over the dielectric stack;

patterning the metallic germanium layer to form a germanium hard mask over the dielectric stack;

etching the dielectric stack through germanium hard mask to form a dielectric hard mask over the major surface of the semiconductor substrate;

etching the semiconductor substrate through the dielectric hard mask;

forming doped regions in the semiconductor substrate; and

forming dielectric and conductive structures over the semiconductor substrate.

Claim 10. (Unchanged) The method as claimed in claim 9, further comprising the step of stripping away the metallic germanium layer after the step of etching the dielectric stack and before the step of etching the semiconductor substrate.

Claim 11. (Unchanged) The method as claimed in claim 10, wherein the step of stripping away the metallic germanium layer includes the steps of:

oxidizing the metallic germanium layer; and

rising the semiconductor substrate in water.

Claim 12. (Unchanged) The method as claimed in claim 9, wherein the step of depositing a metallic germanium layer includes depositing the metallic germanium layer having a thickness between approximately 40 nm and approximately 500 nm in a chemical vapor deposition process.

Claim 13. (Unchanged) The method as claimed in claim 9, wherein the step of patterning metallic germanium layer further includes the steps of:

depositing a photo resist layer over the metallic germanium layer;

exposing and developing the photo resist layer to form a photolithography image; and

etching the metallic germanium layer through the photolithography image.

Claim 14. (Unchanged) The method as claimed in claim 9, wherein the step of forming a dielectric stack further includes the steps of:

forming a pad oxide layer having a thickness between approximately 5 nm and approximately 30 nm on the major surface of the semiconductor substrate;

depositing a nitride layer having a thickness between 50 nm and approximately 300 nm on the pad oxide layer; and

depositing a mask oxide layer having a thickness between 800 nm and approximately 3000 nm on the nitride layer.

Claim 15. (Unchanged) A method for etching a semiconductor wafer, the semiconductor wafer having a dielectric stack over a major surface thereof, the method comprising the steps of:

[providing the semiconductor wafer having a major surface;

forming a dielectric stack over the major surface of the semiconductor wafer;]

forming a germanium hard mask over the dielectric stack;

etching the dielectric stack through germanium hard mask to form a dielectric hard mask over the major surface of the semiconductor wafer; and

etching the semiconductor wafer through the dielectric hard mask.

Claim 16. (Unchanged) The method as claimed in claim 15, wherein the step of forming a germanium hard mask includes the steps of:

depositing a layer of metallic germanium having a thickness equal to or greater than approximately 40 nm over the dielectric stack;

patterning the layer of metallic germanium to form the germanium hard mask.

Claim 17. (Unchanged) The method as claimed in claim 16, wherein the step of patterning the layer of metallic germanium further includes the steps of:

depositing a photo resist layer over the layer of metallic germanium;

patterning the photo resist layer to form a photolithography mask; and

etching the layer of metallic germanium through the photolithography mask.

Claim 18. (Unchanged) The method as claimed in claim 16, further comprising the step of stripping away the germanium hard mask after etching the dielectric stack and before etching the semiconductor wafer.

Claim 19. (Unchanged) The method as claimed in claim 18, wherein the step of stripping away the germanium hard mask includes the steps of:

oxidizing the layer of metallic germanium to convert the layer of metallic germanium into a layer of germanium oxide; and

removing the layer of germanium oxide.

Claim 20. (Unchanged) The method as claimed in claim 19, wherein the step of removing the layer of germanium oxide includes rising the semiconductor wafer in water.

Claim 21. (New) The method as claimed in claim 1, wherein the step of patterning the layer of metallic germanium comprises:

depositing a layer of photo resist;

etching the metallic germanium layer through the layer of photo resist; and

removing the layer of photo resist prior to the step of selectively etching the dielectric layer through the germanium hard mask

Paragraph beginning at page 5, line 16:

Next, metallic germanium layer 22 is [etched] patterned by etching through the photolithography image formed by photo resist layer 24. A reactive ion etching (RIE) process is preferably used to etch metallic germanium layer 22. Other etching process having a high etch selectivity between metallic germanium and photo resist can also be used to etch metallic germanium layer 22 through the mask formed by photo resist layer 24. Because of high the etch selectivity of metallic germanium relative to photo resist, photo resist layer 24 can be a thin layer of photo resist material. The thickness of photo resist layer 24 can further reduced by using a thin layer 22 of metallic germanium, thereby shortening the metallic germanium etching process. A thin photo resist mask is compatible with a shallow depth of focus photolithography processes, and therefore is preferred in the fabrication of semiconductor devices with small features. After etching layer 22 of metallic germanium, photo resist layer 24 is stripped away using techniques known in the art. The remaining germanium serves as a metallic germanium hard mask 25 over of dielectric stack 15 as shown in FIG. 3. Germanium hard mask 25 has openings, e.g., openings 26 shown in FIG. 3, through which dielectric stack 15 is selectively etched in a subsequent step of the etching process.

Paragraph beginning at page 6, line 23:

After oxidation, germanium oxide layer 27 can be removed or stripped from substrate 10 by rinsing substrate 10 or the semiconductor wafer that includes substrate 10 with water. After germanium oxide layer 27 is stripped from the top of dielectric stack 15 over substrate 10, dielectric stack 15 serves as dielectric hard mask 35 (shown in FIG. 6) for subsequently etching semiconductor substrate 10, as shown in Figure 7. To form semiconductor devices [(not shown)] 37 (shown in Figure 8) such as, for example, field effect transistors, bipolar transistors, etc., on semiconductor substrate 10, other processing steps are performed after etching semiconductor substrate 10 through dielectric hard mask 35. These steps include, but are not limited to, forming doped regions in semiconductor

substrate 10 through implantation and/or diffusion; forming dielectric structures over semiconductor substrate 10 through oxidation, deposition, and etching; and forming conductive structures over semiconductor substrate 10. These and other process steps for forming semiconductor devices on substrate 10 are known to those skilled in the art.